

(19)



Europäisches Patentamt  
European Patent Office  
Office européen des brevets



(11)

EP 1 170 671 A1

(12)

## EUROPEAN PATENT APPLICATION

(43) Date of publication:  
09.01.2002 Bulletin 2002/02

(51) Int Cl.7: G06F 17/13

(21) Application number: 00830467.7

(22) Date of filing: 04.07.2000

(84) Designated Contracting States:  
AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU  
MC NL PT SE  
Designated Extension States:  
AL LT LV MK RO SI

- Occhipinti, Luigi  
97100 Ragusa (IT)
- Branciforte, Marco  
95125 Catania (IT)
- Di Bernardo, Giovanni  
95030 Mascalucia (CT) (IT)

(71) Applicant: STMicroelectronics S.r.l.  
20041 Agrate Brianza (Milano) (IT)

(74) Representative: Botti, Mario  
Botti & Ferrari S.r.l. Via Locatelli, 5  
20124 Milano (IT)

(72) Inventors:  
• Arena, Paolo  
95030 Gravina di Catania (IT)

## (54) Programmable analog array circuit

(57) The invention relates to an integrated cellular network structure, being programmable to solve partial derivative differential equations in order to control a phenomenon of diffusion or a propagation of electric drive pulses for robot actuators. Advantageously, such structure comprises analog and digital portions interconnect-

ed with each other; the analog portion includes a matrix array (6) of analog cells (2) arranged to receive data from an I/O interface (7), and the digital portion includes first and second memory arrays (8,9) for storing a desired configuration and the initial state of such analog matrix array (6), respectively.

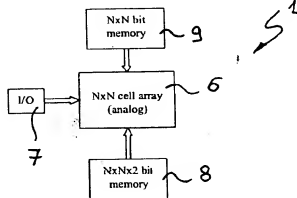


Fig. 3

**Description**Field of the Invention

[0001] The present invention relates to an integrated cellular network structure which can be programmed to solve partial derivative differential equations.

[0002] In particular, the invention relates to an integrated cellular network structure which can be programmed to solve partial derivative differential equations in order to control a phenomenon of diffusion or propagation of electric drive pulses for robot actuators.

Prior Art

[0003] Reported in the pertinent literature are several examples of possible realisations of single-layer cellular neural networks primarily intended for the real-time processing of images.

[0004] By way of example the report of the conference MicroNeuro '99, "CNNUC3: A Mixed-Signal 64x64 CNN Universal Chip" by G. Linan, S. Espejo, R. Domínguez-Castro, E. Roca, A. Rodríguez-Vasquez, is reported among such several examples.

[0005] Another noteworthy prior solution to perform a single-layer cellular neural network is disclosed in the US Patent N. 5,140,670 to L. O. Chua and J. Yang.

[0006] Although in many ways advantageous and substantially achieving their objectives, these prior solutions are limited in applicability and difficult to adapt to the processing of partial derivative differential equations of the second order.

[0007] Research work in electronics and in physics of semiconductors is aimed at developing CMOS technology integrated systems which can solve, in real time, a particular type of second-order partial derivative differential equations, known as reaction-diffusion equations.

[0008] The importance of such equations derive from the biological research, and especially from the study of nervous tissues, where many phenomena of wave-propagation have been detected which can be readily described with mathematical models of the reaction-diffusion type. Besides the biological field, there are numerous phenomena, such as chemical reactions, combustion, etc., that exhibit the same characteristics.

[0009] As described in many documents, particularly in the European Patent Application N. 0 997 235 in the name of the same applicant, cellular neural networks have turned to be excellent tools for solving such equations, though not in their most traditional known versions.

[0010] The underlying technical problem of the present invention is to provide an analog and digital cellular neural network integrated circuit structure with such structural and functional features as to allow partial derivative differential equations to be generated and controlled, and the network initial conditions and control parameters to be programmed.

Summary of the Invention

[0011] The principle of this invention is to provide a network wherein the values of the parameters of equations to be generated can be defined, and the form of the structure re-defined. Thus, the whole available array or just one or a few portions thereof can be used with different parameters and forms. Also, since the phenomena to be generated may have different time constants, the typical frequency of an individual cell can be varied within a broad range (1MHz to 1Hz).

[0012] Furthermore, the invention is very different from conventional cellular neural networks not only by its structure but also in the respect of its programmability.

[0013] The features and advantages of an integrated structure according to the invention will be apparent in the following description of an embodiment thereof, given by way of example and not of limitation with reference to the accompanying drawings.

Brief Description of the Drawings**[0014]**

- Figures 1A and 1B show schematic views showing the dynamic with respect to the phases and the time domain for the state variables of a generic analog cell incorporated in the integrated structure according to the present invention.
- Figure 2 shows a schematic view showing simplified blocks of the circuit architecture of an individual program-

mable cell in its parameters and in its initial state, according to the invention.

- Figure 3 is a schematic block diagram of an integrated, programmable cellular network structure according to this invention.
- Figures 4 and 5 show schematic views showing circuitual blocks of the integrated structure according to the invention.
- Figure 6 shows a detail view of the cell structure shown in Figure 2.
- Figures 7A and 7B show diagrams of response vs. time constant of the inventive structure.
- Figure 8 shows one embodiment of a portion of the cell structure of Figure 2.
- Figure 9 shows a more detailed schematic view of a circuit portion of the cell 2.
- Figures 10 and 11 schematically show further embodiments.
- Figure 12 shows an electric diagram of a transconductance circuit implementing a detail of the cell of Figure 2.
- Figure 13 shows a diagram of a characteristic curve of the circuit of Figure 12.
- Figure 14 shows an electric diagram of a further detail of the cell shown in Figure 2.
- Figures 15A and 15B show diagrams of characteristic curves of elements provided in the cell of Figure 2.
- Figure 16 is a photograph of a driven belt conveyor of the circuitual structure of this invention, taken during its transport action.

#### Detailed Description

[0015] With reference to the drawing views, specifically to the example of Figure 3, an programmable cellular network integrated structure according to this invention is generally shown at 1 in schematic form.

[0016] The structure 1 comprises a plurality of cells 2 arranged into an NxN matrix, as described hereinafter in relation to Figure 2.

[0017] More particularly, the invention relates to a cellular network integrated structure 1 which can be programmed to solve partial derivative differential equations in order to control a phenomenon of electric drive pulse diffusion or propagation to robot actuators. The structure 1 comprises an analog portion and a digital portion interconnected to each other.

[0018] The analog portion comprises a matrix array 6 of analog cells 2 arranged to receive data from an I/O interface 7, and the digital portion comprises first and second memory arrays 8 and 9 for storing up a desired configuration and the initial state, respectively, of the analog array 6.

[0019] The basic mathematical model of an individual cell 2 is represented by a system of partial derivative equations of the second order as described in expression (1) below:

$$\begin{aligned} dX1_{i,j}/dt = & -X1_{i,j} + (1+\mu+\epsilon)Y1_{i,j} - s1 Y1_{i,j} + D1(Y1_{i-1,j} + Y1_{i+1,j} + Y1_{i,j-1} + \\ & + Y1_{i,j+1} - 4 Y1_{i,j}) \end{aligned} \quad (1)$$

$$\begin{aligned} dX2_{i,j}/dt = & -X2_{i,j} + (1+\mu+\epsilon)Y2_{i,j} - s2 Y2_{i,j} + D2(Y2_{i-1,j} + Y2_{i+1,j} + Y2_{i,j-1} + \\ & + Y2_{i,j+1} - 4 Y1_{i,j}) \end{aligned} \quad (2)$$

$$Yk_{i,j} = 0,5(IXk_{i,j} + 1I - IXk_{i,j} - 1I) \quad (3)$$

[0020] For particular parameter values, the state variables in the above system of equations describe a borderline cycle characterised by a slow-fast dynamic, that is a dynamic wherein two separate dynamic processes coexist which have deeply different kinetic characteristics.

[0021] Figures 1A and 1B show the dynamic with respect to the phases and the time domain for the state variables of a generic cell.

[0022] These dynamics produced by the individual cells, in combination with a phenomenon of diffusion between cells, result in an overall behaviour which can be likened to a reaction-diffusion process exhibiting similar characteristics in several chemio-physical phenomena, as well as in the propagation of self-supporting waves for transport purposes.

[0023] An object of this invention is to provide an integrated programmable device which can generate electric pulses for driving such phenomena in order to control locomotion actuators, e.g. the actuators disclosed in the European Patent Application N. 0 997 235 in the name of the same Applicant.

[0024] "Programming" such devices means pre-arranging a suitable set of initial and boundary conditions, both as relates to programming the characterising parameters of an individual cell or to re-configuring the structure of the cell matrix array, as well as the possibility of changing the time constant of each cell.

[0025] To integrate the functions of a circuit architecture of the aforementioned type in a single device on silicon, one possible monolithic circuitual implementation will be considered by way of example, without this being limitative of the invention scope.

[0026] Figure 2 shows a simplified block diagram of the architecture of an individual cell 2 whose parameters and initial state can be programmed in accordance with the invention, as previously outlined.

[0027] The cell 2 comprises an analog core 3 and a set of registers wherein the values of the equation parameters and of the initial conditions are stored in a digital format. Interaction between the analog portion 3 of the structure and the digital portion 4 is afforded by suitable circuits 5, to be described, realising a so-called scaling of a current value according to a constant factor which is contained in the registers, to thus obtain a multiplication of such current, define the parameters of the equation to be solved, and convert said current to a voltage for setting the initial conditions. From a purely applicational standpoint, setting these initial conditions is to apply appropriate voltage values to selected capacitors.

[0028] Figure 3 shows a schematic view of the integrated structure 1 of a programmable cellular network according to the invention, which comprises:

an NxN array 6 of cells 2 similar to that described with reference to Figure 2;

an interface I/O block 7 adapted for input/output data buffering;

at least first 8 and second 9 structurally independent non-volatile memories, with the size of the first 8 being NxNx2 bits and that of the second 9 being NxN bits.

[0029] The first 8 of such memories can store a desired configuration of the array 6; the second memory 9 is used to set the state of a given cell at a desired value.

[0030] Figures 4 and 5 schematically show two possible implementations of the cell 2, in which the correspondence of the previously discussed theoretical blocks of the diagram of Figure 2 with the actual blocks of the hardware structure can be appreciated.

[0031] The data inputs and outputs of an individual analog cell 2 are also obtainable from the Figures.

[0032] All of the blocks comprised in the two possible implementations of Figures 4 and 5 will now be briefly and qualitatively described, the blocks regarded to be the most important and innovative being discussed in detail later in this specification.

[0033] The [Init.Cond.] block 10 is to set pre-fixed conditions for the system at an initial time (zero time). Essentially, the block 10 sets desired voltage values at the head of capacitors comprised in the cell 2.

[0034] The [ $\tau$ ] block 11 represents the system time constant, which can be varied within a broad range by changing the system own frequency.

[0035] The [N.L.] block 12 is effective to reproduce the non-linearity of the equation to be represented.

[0036] The [Laplaciano] block 13 handles the interactions between the cells 2 in the array 6.

[0037] The [ $i_1, i_2$ ] blocks 14 and 15 are just current generators.

[0038] The [ $1+\mu+e, 1+\mu+e, s_1, s_2$ ] blocks 16, 17, 18 and 19 are current multipliers controlled by digital signals.

[0039] Advantageously in this invention, full versatility of the system is achieved by varying the time constant of the individual cell 2, since different applications require radically different working frequencies, e.g. of a few Hertz to thousands of Hertz.

[0040] The simplest way of varying the parameter  $\tau$  is to change the values of the capacitances C1, C2 comprised in the diagram of the cell 2. However, the time constant  $\tau$  of the system is held in the 100kHz range because of tech-

nological constraints.

[0041] According to the invention, to lower the typical frequency of the cell 2 in a simple way, two switches 29, 32 are provided for use between the capacitances C1, C2 and their corresponding resistors R, each switch being contained in its corresponding block 11 as shown in Figure 2. Figure 6 shows an enlarged view of the circuit portion extending between one of the capacitances C1 or C2 and one of the resistors R, which portion containing one of the frequency switches.

[0042] The switches 29, 32 are also operative to isolate the capacitances from the rest of the circuit structure.

[0043] When the switches 29, 32 are closed, the system evolves, whereas when the switches are open, the system conditions are "frozen". These switches are required to stay open for a much shorter time than the discharge time of the capacitances C1, C2.

[0044] Thus, the same curves can be obtained with different frequencies, as shown in Figures 7B and 7A illustrating the system response to a variation of the time constant.

[0045] With this method, the time constant can even be multiplied by a factor 100k to obtain frequencies in the range of one Hertz.

[0046] The digital-controlled block 10 is arranged to set the individual cells 2 at desired initial conditions, the block 10 outputting a voltage which is proportional to the binary digit stored in a suitable register, which may be a 4-bit register, for example.

[0047] Shown in Figure 8 is an exemplary embodiment of the block 10, which allows to a current-to-voltage conversion.

[0048] The structure of a cell 2 is completed by a pair of switches 20, 21, each associated with a corresponding capacitance C1, C2 of the cell 2. These switches 20, 21 are operative to isolate each of the capacitances C1, C2 from the block 10 output.

[0049] The switches 20 and 29 are suitably set in opposite phases with each other, as well as the switches 21 and 32.

[0050] Figure 9 shows a more detailed view of the circuit portion of Figure 2 for setting the initial conditions. The network 25 of logic gates 26, 27 and 28 handling a reset signal is also more clearly visible.

[0051] The Laplacian block 13 includes two functional portions 30 and 31, having a mode of operation that will be hereafter described.

[0052] To create particular sub-matrices or vectors or paths inside the matrix array of cells 2, the following addends in equations (1) and (2) need to be modified, which represent the cell interaction terms:

$$D1 (Y1_{i,j-1} + Y1_{i+1,j} + Y1_{i,j-1} + Y1_{i,j+1} - 4 Y1_{i,j}) \quad (4)$$

$$D2 (Y2_{i,j-1} + Y2_{i+1,j} + Y2_{i,j-1} + Y2_{i,j+1} - 4 Y2_{i,j}) \quad (5)$$

[0053] More particularly, when one cell is to be disconnected from an adjacent cell, it is sufficient to eliminate the corresponding output value from the relations (4) and (5), and to decrease by one the feedback factor 4.

[0054] This can be done by means of the circuit blocks 37 and 39, shown in Figures 10 and 11, respectively.

[0055] The block 37 represents an exemplary circuit embodiment of the block 30 inside the Laplacian block 13. Such block 37 is operative to add together the desired currents of the neighbouring cells (Sum) and to multiply the output variables of the neighbouring cells by the diffusion factor (Dk).

[0056] The block 39 represents indeed an exemplary circuit embodiment of the block 31 inside the Laplacian block 13, and is operative to multiply the output variable by either a factor A or an integer factor between 0 and 4.

[0057] Both blocks 37 and 39 are completed by digital current multipliers in order to obtain the product of the summation and the factors Dk.

[0058] Shown in Figure 11 are also reference numerals to circuit portions 38 and 40 to be described.

[0059] To obtain the non-linear function represented by the block 12 and shown in the equation defining the behaviour of an individual cell, a saturated transconductance amplifier 41 may be used, for example. A circuit diagram of this amplifier 41 is given in Figure 12. The amplifier 41 essentially comprises a differential stage, so that a sigmoid ( $\Sigma$ -shaped) curve can be obtained, later to be clipped by two constant currents.

[0060] Figure 13 is a plot of voltage vs. current illustrating the transcharacteristic function 42 of the transconductance circuit 41 of Figure 12.

[0061] A further peculiarity for consideration is a resistive element R provided in each cell layer as shown in Figure 2. The gradient of the characteristic curve of this element should be equal to that of the middle portion of the characteristic curve of the non-linear element, in connection with the phenomenon to be reproduced. In view of the tolerances of current technology resistive elements, problems of the two gradients disagreeing with each other might be encountered.

[0062] To obviate this, the resistive element can be seen as a linear function of the voltage applied at its heads, subtracting current from the summing node of Figure 2, and can therefore be substituted by a transconductor drawing current from that node.

[0063] In such a way, the same characteristic function can be used by clipping it with two constant currents, similar as in the previous embodiment, so as to create the non-linear block 12. In this way, the gradients of both curves can be made to agree, and the system relieved of constraints from the tolerances of its constituent elements.

[0064] An exemplary circuit illustrating this possibility is shown in Figure 14, where the circuit 35 represents the embodiment of a modified or corrected gradient transconductor.

[0065] Shown in Figures 15A and 15B are examples of this possible embodiment. Curves 43 and 44 show the gradients of the resistive element and the corrected gradient transconductance element, respectively.

[0066] Advantageously, the principle of this invention can be applied to industrial automation and robotic. The absence of reflective phenomena in the generation and propagation of auto-waves prevents noise formation, and makes the inventive approach particularly suitable for the construction of transportation supports and aids.

[0067] The "in-line" programmability of the inputs provides sophisticated direction control by allowing, for example, several objects laid onto a belt conveyor designed with this philosophy to be routed along different directions according to necessity, without any actions on the belt conveyor itself being required.

[0068] Figure 16 shows, by way of example, a prototype of a belt conveyor capable of transporting an object, here a small ball, from a fixed station to another desired station, according to a diffusive control as described hereinabove.

[0069] Of course, the invention also allows the development of robot architectures, which have an analog locomotion system inspired by biological deambulation.

[0070] A six-limbed robot prototype has been made by the Applicant. Such prototype is able to independently move by means of an auto-wave propagation. This auto-wave is generated by a discrete element circuit structure whereby the propagation of a wave can be activated on a cell vector from which the self-propagating wave is picked up to directly drive the robot servos.

[0071] Thus, the invention allows the realisation of a cellular network circuit integrated architecture adapted to solve partial derivative differential equation, whereby electrical signals can be picked up, such signals having the typical periodicity of physical phenomena, such as auto-waves used to drive robot architectures able to independently move.

[0072] In addition, a number of this invention's features make it specially suitable for a variety of applications, such as:

- 1) a re-configurable network, meaning feasibility of an array of cells 2 which can be used as a whole or in one or more subassemblies (vectors, subarrays, special patterns, etc.);
- 2) programmability, meaning the faculty to set the structure, the parameters, and the initial conditions of the array.

## Claims

1. An integrated cellular network structure, being programmable to solve partial derivative differential equations in order to control a phenomenon of diffusion or a propagation of electric drive pulses for robot actuators, **characterised in that** it comprises analog and digital portions interconnected to each other, with said analog portion including a matrix array (6) of analog cells (2) arranged to receive data from an input/output interface (7), and said digital portion including a first and a second memory matrix arrays (8,9) arranged to store a desired configuration and the initial state, respectively, of said analog matrix array (6).
2. An integrated structure according to Claim 1, **characterised in that** said memory matrix arrays (8,9) are structurally independent.
3. An integrated structure according to Claim 1, **characterised in that** it comprises in the analog matrix array (6) a block (10) connected to said interface (7) for setting predetermined initial conditions to the structure.
4. An integrated structure according to Claim 3, **characterised in that** said predetermined initial conditions comprise setting potential values for capacitors (C1,C2) contained in the analog matrix array (6).
5. An integrated structure according to Claim 1, **characterised in that** the cells (2) of the analog matrix array are two-layer cells.
6. An integrated structure according to Claim 4, **characterised in that** each analog cell (2) includes a block (11) having a variable time constant for individually modifying the frequency of each cell (2).

7. An integrated structure according to Claim 6, **characterised in that** said time constant block (11) comprises at least one switch (29,32) for releasably connecting each capacitor to corresponding resistors (R).
8. An integrated structure according to Claim 1, **characterised in that** said analog cell (6) includes current multipliers (16,17,18,19) driven by digital signals.
9. An integrated structure according to Claim 1, **characterised in that** each cell (2) includes at least a Laplacian block (13) operative to control the interaction between adjacent cells (2) of the analog matrix array (6).
10. An integrated structure according to Claim 1, **characterised in that** it solves the following differential equations:

$$\begin{aligned} dX1_{i,j}/dt = & -X1_{i,j} + (1+\mu+\epsilon)Y1_{i,j} - s1 Y1_{i,j} + D1(Y1_{i-1,j} + Y1_{i+1,j} + Y1_{i,j-1} + \\ & + Y1_{i,j+1} - 4 Y1_{i,j}) \end{aligned} \quad (1)$$

$$\begin{aligned} dX2_{i,j}/dt = & -X2_{i,j} + (1+\mu+\epsilon)Y2_{i,j} - s2 Y2_{i,j} + D2(Y2_{i-1,j} + Y2_{i+1,j} + Y2_{i,j-1} + \\ & + Y2_{i,j+1} - 4 Y1_{i,j}) \end{aligned} \quad (2)$$

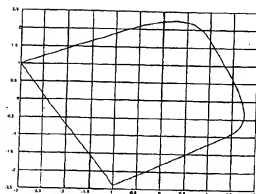


Fig. 1A

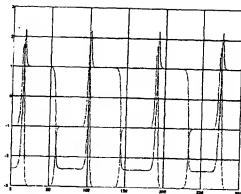


Fig. 1B

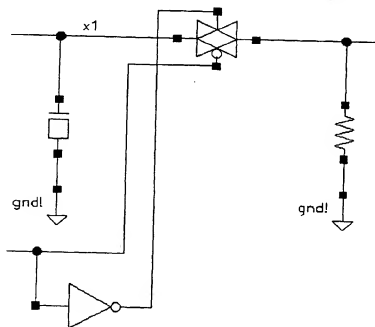


Fig. 6



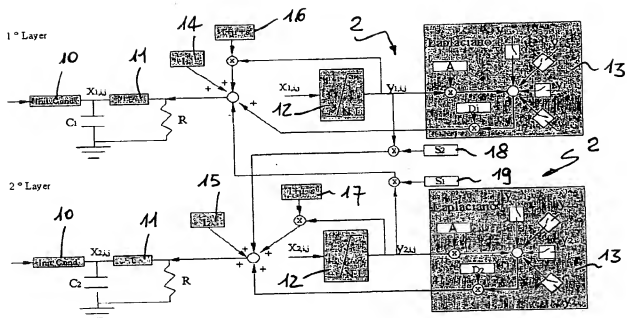


Fig. 2

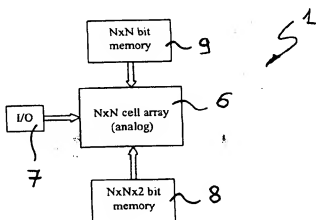


Fig. 3

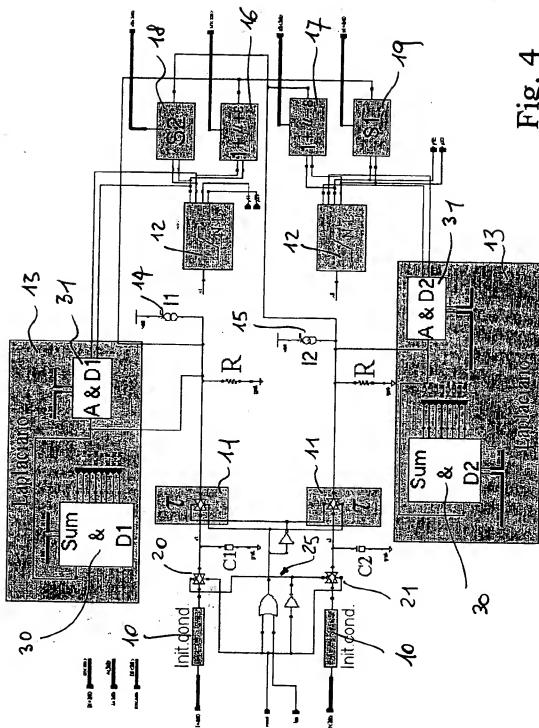
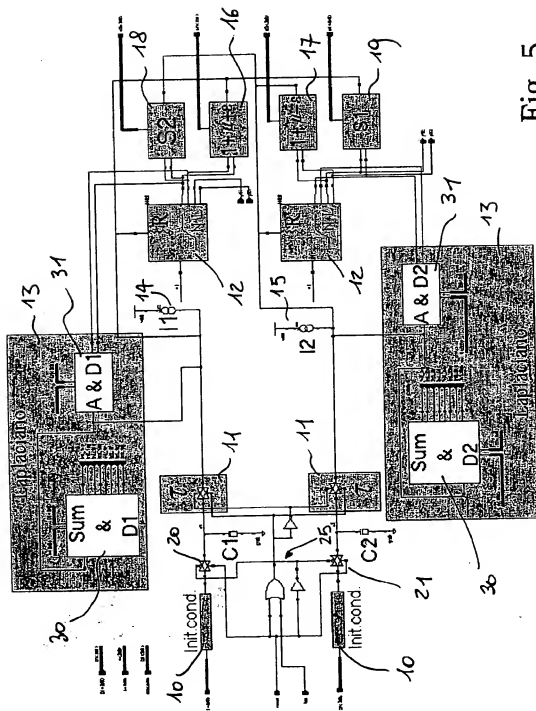


Fig. 4



5  
Firm

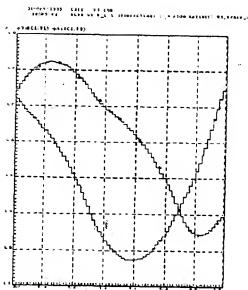


Fig. 7B

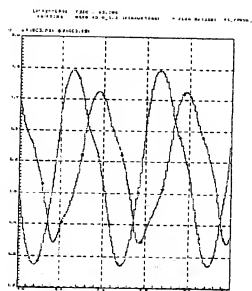


Fig. 7A

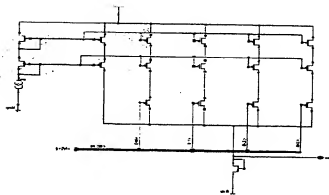


Fig. 9

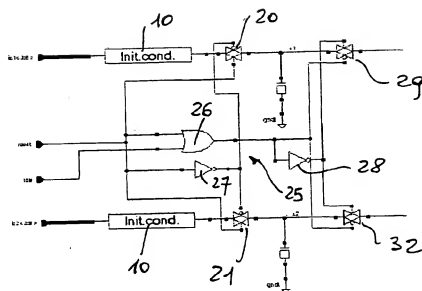
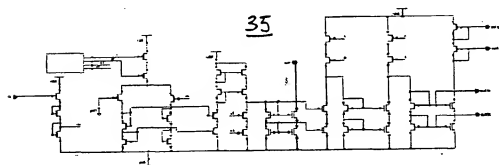


Fig. 14



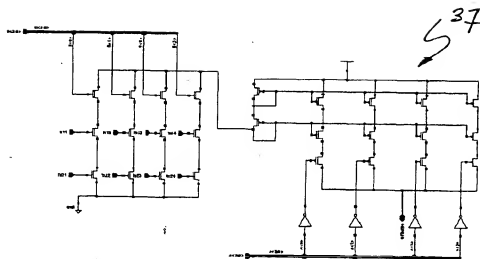


Fig. 10

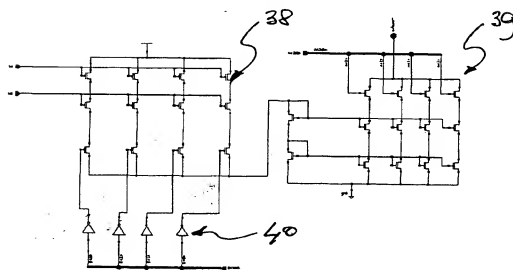


Fig. 11

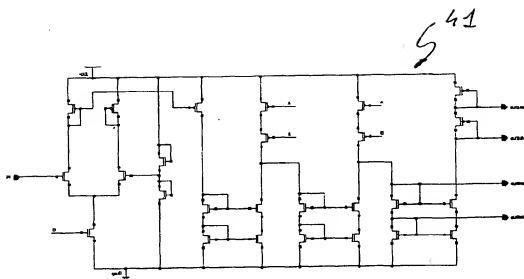


Fig. 12

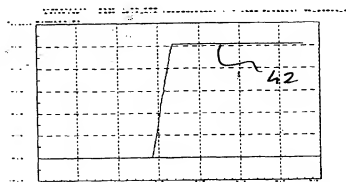


Fig. 13

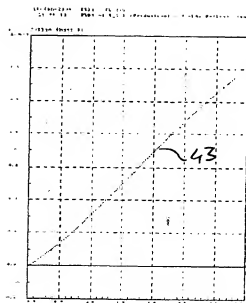


Fig. 15A

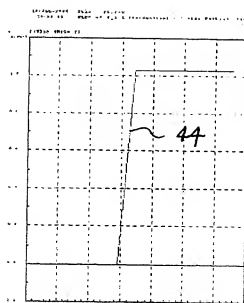


Fig. 15B

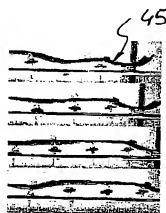


Fig. 16





European Patent  
Office

## EUROPEAN SEARCH REPORT

Application Number  
EP 00 83 0467

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Incl. C17)
X	ARENA P ET AL: "Reaction-diffusion CNN chip. I. IC implementation" 2000 IEEE INTERNATIONAL SYMPOSIUM ON CIRCUITS AND SYSTEMS. EMERGING TECHNOLOGIES FOR THE 21ST CENTURY. PROCEEDINGS (IEEE CAT NO. 00CH36353), ISCAS 2000 GENEVA. 2000 IEEE INTERNATIONAL SYMPOSIUM ON CIRCUITS AND SYSTEMS. EMERGING TECHNOLOGIES FOR THE 21ST CENTURY. 419-422 vol.3, XP000965128 2000, Lausanne, Switzerland, Presses Polytech. Univ. Romandes, Switzerland ISBN: 0-7803-5482-6 * the whole document *	1-10	G06F17/13
X	US 5 691 664 A (BERSCH DANNY A ET AL) 25 November 1997 (1997-11-25) * claims 1,6; figure 1 *	1-10	
A	US 5 680 070 A (GARRITY DOUGLAS A ET AL) 21 October 1997 (1997-10-21)		TECHNICAL FIELDS SEARCHED (Incl. C17)
A	ARENA P ET AL: "Reaction-diffusion CNN chip. II. Applications" 2000 IEEE INTERNATIONAL SYMPOSIUM ON CIRCUITS AND SYSTEMS. EMERGING TECHNOLOGIES FOR THE 21ST CENTURY. PROCEEDINGS (IEEE CAT NO. 00CH36353), ISCAS 2000 GENEVA. 2000 IEEE INTERNATIONAL SYMPOSIUM ON CIRCUITS AND SYSTEMS. EMERGING TECHNOLOGIES FOR THE 21ST CENTURY. 427-430 vol.3, XP000964669 2000, Lausanne, Switzerland, Presses Polytech. Univ. Romandes, Switzerland ISBN: 0-7803-5482-6 --- -/--		G06F H03K
The present search report has been drawn up for all claims			
Place of search		Date of completion of the search	Examiner
THE HAGUE		21 November 2000	Pierfederici, A
CATEGORY OF CITED DOCUMENTS			
X: particularly relevant if taken alone Y: particularly relevant if combined with another document of the same category A: technological background O: non-written disclosure P: intermediate document		T: theory or principle underlying the invention E: earlier patent document, but published on, or after the filing date D: document cited in the application L: document cited for other reasons & : number of the same patent family, corresponding document	

EP 00 83 0467 (P)



European Patent  
Office

# EUROPEAN SEARCH REPORT

Application Number  
EP 00 83 0467

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Incl.7)
A	<p>ARENA P ET AL: "Autowaves for motion control: a CNN approach"            ISCAS '98. PROCEEDINGS OF THE 1998 IEEE INTERNATIONAL SYMPOSIUM ON CIRCUITS AND SYSTEMS (CAT. NO.98CH36187), ISCAS '98 PROCEEDINGS OF THE 1998 IEEE INTERNATIONAL SYMPOSIUM ON CIRCUITS AND SYSTEMS, MONTEREY, CA, USA, 31 MAY-3 JUNE 1998, pages 163-166 vol.3, XP002153385            1998, New York, NY, USA, IEEE, USA            ISBN: 0-7803-4455-3            -----</p>		
			TECHNICAL FIELDS SEARCHED (Incl.7)
The present search report has been drawn up for all claims			
Place of search <b>THE HAGUE</b>		Date of completion of the search <b>21 November 2000</b>	Examiner <b>Pierfederici, A</b>
CATEGORY OF CITED DOCUMENTS		T: theory or principle underlying the invention E: earlier patent document, but published on, or after the filing date D: document cited in the application I: document cited for other reasons A: technological background O: non-written disclosure P: intermediate document a: member of the same patent family, corresponding document	
X: particularly relevant if taken alone Y: particularly relevant if combined with another document of the same category A: technological background O: non-written disclosure P: intermediate document			

EPO FORM 183 (3/92) (P/0001)

ANNEX TO THE EUROPEAN SEARCH REPORT  
ON EUROPEAN PATENT APPLICATION NO.

EP 00 83 0467

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

21-11-2000

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5691664 A	25-11-1997	NONE	
US 5680070 A	21-10-1997	NONE	

EPO/COM/POUR

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82

**THIS PAGE BLANK (USPTO)**

**This Page is Inserted by IFW Indexing and Scanning  
Operations and is not part of the Official Record**

**BEST AVAILABLE IMAGES**

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images include but are not limited to the items checked:

- ☐ BLACK BORDERS
- ☐ IMAGE CUT OFF AT TOP, BOTTOM OR SIDES
- ☒ FADED TEXT OR DRAWING
- ☒ BLURRED OR ILLEGIBLE TEXT OR DRAWING
- ☐ SKEWED/SLANTED IMAGES
- ☐ COLOR OR BLACK AND WHITE PHOTOGRAPHS
- ☐ GRAY SCALE DOCUMENTS
- ☒ LINES OR MARKS ON ORIGINAL DOCUMENT
- ☐ REFERENCE(S) OR EXHIBIT(S) SUBMITTED ARE POOR QUALITY
- ☐ OTHER: \_\_\_\_\_

**IMAGES ARE BEST AVAILABLE COPY.**

As rescanning these documents will not correct the image problems checked, please do not report these problems to the IFW Image Problem Mailbox.

**THIS PAGE BLANK (USPTO)**